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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
CAMPBELL, SHAUN M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,305	TANAKA ET AL.	
	Examiner	Art Unit	
	SHAUN CAMPBELL	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/14/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

1. Claims 18-34 are presented for examination. Claims 1-17 are canceled and claims 18-34 are new.

Specification

2. The abstract of the disclosure is objected to because extensive mechanical and design details of apparatus should not be given. Please delete the reference numbers from the abstract. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 18-26, 29, 30, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami et al. (US Patent No. 7,036,741 B2, hereafter referred to as Usami) in view of Yamakawa (US Patent No. 6,479,777 B2).

6. As to claims 18-24, 30 and 34, Usami discloses a manufacturing method for an electronic device that has IC elements (fig 2A, IC chip 16), each IC element having electrodes formed respectively on the respective surfaces of a pair of opposed sides thereof (fig 2A, electrodes 13 and 17), and a first circuit layer (fig 2B, 1st metal conductor 14 on upper substrate 12) and a second circuit layer (fig 2B, 2nd metal conductor 18 on lower substrate 19), comprising:

a step of forming a slit (fig 3, slit 22a and col. 11, lines 29-35) in the first circuit layer or the second circuit layer;

a step of forming a first connecting part for electrically connecting the electrode of one side of the IC elements and the first circuit layer, on the one side (fig 2B, electrode 13), a second connecting part for electrically connecting the electrode of the other side of the IC elements and the second circuit layer (fig 2B, electrode 17), and a third connecting part for electrically connecting the first and second circuit layers so that the second connecting part and the third connecting part are connected spanning the slit (fig 2D, conductor-connection portion 20); and

a step of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers (fig 15A, upper substrate 12h is aligned with lower substrate 19h using sprocket holes 141 and the chip is sandwiched between, col. 18, lines 33-42).

Usami does not explicitly disclose continuously supplying the IC elements individually into an IC elements transport mechanism [claim 18-23].

Nonetheless, Yamakawa discloses continuously supplying the IC elements individually into an IC elements transport mechanism (fig 1 and col. 5, lines 1-8)[claim 18].

wherein the step of continuously supplying the IC elements comprises:

a step of individually holding an IC element (fig 2, electronic parts 2) in an IC element holding part (slots 2) of an IC elements transport mechanism (table 1) having not less than one IC element holding part (slots 2); and

a step of delivering the IC element thus held by running the IC element holding part of the transport mechanism (col. 4, lines 29-67)[claim 19];

a step of individually holding an IC element in an IC element holding part of a disc shaped IC elements transport mechanism (fig 2, disk-shaped conveying table 1) having not less than one IC element holding part [claim 20];

a step of individually holding an IC element in an IC element holding part of an IC elements transport mechanism having not less than one IC element holding part which is formed as a notch shape (fig 2, slots 2)[claim 21];

a step of aligning the IC elements by action of an IC elements alignment/supply mechanism (fig 1, feed device 15 and linear track 15a) to facilitate individually holding an IC element in an IC element holding part of an IC elements transport mechanism having not less than one IC element holding part [claim 22];

a step of aligning the IC elements by action of an IC elements alignment/supply mechanism which is a line feeder (fig 1, feed device 15 and linear track 15a) to facilitate individually holding an IC element in an IC element holding part of an IC elements transport mechanism having not less than one IC element holding part [claim 23];

Yamakawa does not explicitly disclose a step of aligning the IC elements by action of an IC elements alignment/supply mechanism which is a high frequency alignment feeder to facilitate individually holding an IC element in an IC element holding part of an IC elements transport mechanism having not less than one IC element holding part [claim 24]. However, Yamakawa does disclose a step of aligning the IC elements by action of an IC elements alignment/supply mechanism (fig 1, feed device 15/15a and table 1) to facilitate individually holding an IC element in an IC element holding part of an IC elements transport mechanism having not less than one IC element holding part (fig 2, slots 2). Therefore Yamakawa discloses the claimed invention except for the alignment feeder runs at a high frequency. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the feeder and table of Yamakawa at a high frequency, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the

optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the electronic parts conveying apparatus, as taught by Yamakawa, in order to continuously supply the IC elements into the sandwich as taught by fig 15A/B and col. 18, lines 33-42 of Usami because testing and sorting the IC elements before completing subsequent manufacturing steps will save the manufacturer the trouble of making chips that do not function properly.

7. As to claim 25, Usami in view of Yamakawa discloses the manufacturing method for an electronic device according to claim 18 (paragraphs above).

Usami further discloses wherein the electrical connection of an electrode of the IC elements and at least one of the first and the second circuit layers is made via an anisotropic conductive adhesive layer (col. 10, lines 53-57).

8. As to claim 26, Usami in view of Yamakawa discloses the manufacturing method for an electronic device according to claim 18 (paragraphs above).

Usami further discloses further comprising: a step of connecting at once, the electrodes of the IC elements and at least one layer from among the first or the second circuit layers, wherein the step of connecting is after the step of positionally aligning the connection surfaces (col. 18, lines 33-42; where it would have been obvious to one of ordinary skill in the art that the sprocket holes are used for alignment).

9. As to claim 29, Usami in view of Yamakawa discloses the manufacturing method for an electronic device according to claim 26 (paragraphs above).

Usami further discloses further comprising: a step of cutting a continuum of a plurality of the IC elements into individual pieces (fig 21E, chip-separation portions 246 and Col. 22, lines 49-52).

However, Usami does not explicitly disclose wherein the step of cutting is after the step of connecting, at once, a plurality of the IC elements with at least one from among the first and the second circuit layers.

Nonetheless, Usami does disclose the step of cutting is after the step of connecting, at once, a plurality of the IC elements with at least one form among the first and the second circuit layers (col. 18, lines 33-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to cut the devices from the tape into individual devices because these devices are usually made to be used individually and the reason for rolling the devices into a tape reel is for the advantage of easy handling of the wireless identification semiconductor devices (col. 18, lines 43-47), therefore it would be obvious to cut the devices as disclosed in fig 21E into individual devices be being used.

10. As to claim 30, Usami further discloses wherein a conductive layer (fig 2B, 1st metal conductor 14) is formed on the surface of at least one from among the first and the second circuit layers (fig 2B, upper substrate 12).

11. As to claim 34, Usami in view of Yamakawa discloses the manufacturing method for an electronic device according to claim 18 (paragraphs above).

Usami further discloses wherein electrical connections of electrodes of the IC elements and the first and second circuit layers are made via first and second anisotropic conductive adhesive layers, respectively (col. 10, lines 53-57).

Usami in view of Yamakawa does not explicitly disclose a total thickness of the first and second anisotropic conductive adhesive layers is not less than half the thickness of the IC elements.

However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the device with a thickness not less than half the thickness of the IC elements, since it was held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

12. Claims 27-28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami in view of Yamakawa, and further in view of Moskowitz et al. (US Patent No. 5,528,222) hereafter referred to as Moskowitz.

13. As to claims 27 and 28, Usami in view of Yamakawa discloses the manufacturing method for an electronic device according to claim 26 (paragraphs above).

Usami in view of Yamakawa does not explicitly disclose wherein the method in that the electrodes of the IC elements and at least one layer from among the first and the second circuit layers are connected at once is realized by thermal compression [claim 27]; or

wherein the gaps between the first and second circuits layers are sealed by the thermal compression [claim 28]. However, Usami does disclose using a pin to seal the gaps between the first and second circuits layers (fig 2C, press pin 21).

Nonetheless, Moskowitz discloses using thermal compression bonding in order to electrically connect circuits to a chip (col. 4, lines 13-16)[claims 27 and 28].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use thermal compression to connect the electrodes to the other circuit layers, since it was known in the art that thermal compression can be used to connect electrodes to other circuit layers.

14. As to claim 31, Usami further discloses wherein the first and second circuit layers include aluminum (col. 5, lines 30-32).

15. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami in view of Yamakawa and Moskowitz as applied to claim 28, and further in view of Green et al. (US Pub No. 2003/0136503 A1) hereafter referred to as Green.

16. As to claims 32 and 33, Usami in view of Yamakawa and Moskowitz disclose the manufacturing method for an electronic device according to claim 28 (paragraphs above).

Usami in view of Yamakawa and Moskowitz does not explicitly disclose wherein at least one from among the first and second circuit layers is supported on a base substrate comprised of an organic resin, and that this organic resin be selected from the group consisting of polyvinyl chloride (PVC), acrylonitrile butadiene styrene (ABS), polyethylene terephthalate (PET), polyethylene terephthalate glycol (PETG), polyethylene naphthalate (PEN), polycarbonate resin (PC), biaxial polyester (O-PET), and polyimide resin [claim 32]; or

wherein either one of the first or the second circuit layer is supported on a base substrate comprised of paper [claim 33].

Nonetheless, Green discloses a base substrate for a RFID webstock containing an semiconductor chips made out of these materials ([0138] lines 1-13)[claim 32] and

wherein the substrate may comprise paper ([0036] lines 7-9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the conventional features of using organic resin or paper as the substrate of Usami in view of Yamakawa and Moskowitz as taught by Green in order for the devices to be easily cut and also have dimensional and thermal stability.

Response to Arguments

17. Applicant's arguments with respect to claims 18-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAUN CAMPBELL whose telephone number is (571)270-3830. The examiner can normally be reached on Monday Through Friday 8:00AM-5:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shaun Campbell/
Examiner, Art Unit 2829
11/19/2008

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829